EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ryan Flax on 1/28/2010.

The application has been amended as follows:

113. (Currently Amended) An imager structure, comprising:

a pixel array having pixels arranged in rows and columns;

said pixel array comprising a first pixel and a second pixel formed in respectively adjacent columns and in conjunction with an active area spanning a first associated photodetector of the first pixel and a second associated photodetector of the second pixel but no other photodetectors <u>of other pixels</u>, said active area having the first associated photodetector and the second associated photodetector at opposite ends of said active <u>area</u> and having a two-dimensional shape as the pixel array is viewed from above; and

a common output for charges generated from the first photodetector and the second photodetector at a portion of said active area between said first and second photodetectors, the common output being coupled to a signal output line shared by the first pixel and the second pixel, wherein the two-dimensional shape of said active area between the first and second associated photodetectors comprises an active area component that extends diagonally ~~is a substantially diagonal shape~~ with respect to an extending direction of said signal output line ~~column line~~ within the pixel array.

114. (Currently Amended) The pixel array of claim 113, wherein the active area ~~shared by the first and second pixels~~ is S-shaped.

115. (Currently Amended) A pixel array, comprising:

a first pixel and a second pixel, the first pixel having a first photodetector and the second pixel having a second photodetector, wherein an active area is shared by only the first photodetector ~~shares an active area with~~ and the second photodetector ~~and no other photodetector~~, said shared active area providing an output for said first and second photodetectors and having a two-dimensional shape as the pixel array is viewed from above; and

a common readout line for receiving a signal from said first and second photodetectors coupled to the active area shared by the first pixel and the second pixel,

wherein the two-dimensional shape of the shared active area between the first and second photodetectors comprises an active area component that extends diagonally ~~is a substantially diagonal shape~~ relative to an extending direction of the common readout line across the pixel array.

117. (Currently Amended) A pixel array, comprising:

a first pixel and a second pixel, said first pixel having a first photodetector and said second pixel having a second photodetector, wherein an active area is shared by only said first photodetector ~~shares an active area with~~ and said second photodetector, ~~and no other photodetector~~ and at least one of said first pixel and said second pixel further comprises a reset transistor, said reset transistor comprising a gate, a first source-drain region, and a second source-drain region in a linear arrangement as viewed from above the pixel array, wherein said shared active area between the first and second photodetectors has a ~~substantially diagonal~~ two-dimensional shape as the pixel array is viewed from above, the two-dimensional shape comprising an active area component that extends diagonally relative to the linear arrangement of the reset transistor as the pixel array is viewed from above; and

a common readout line for receiving charge from said shared active area.

The following is an examiner's statement of reasons for allowance:

Allowable Subject Matter

Claims 113-123 allowed.

Regarding claim 113, Hashimoto discloses, **"a pixel array having pixels arranged in rows and columns"**, as exhibited in figure 10.

In addition, Hashimoto discloses, **"said pixel array comprising a first pixel and a second pixel formed in respectively adjacent columns and in conjunction with an active area spanning a first photodetector of the first pixel and a second photodetector of the second pixel but no other photodetectors of other pixels, said active area having the first associated photodetector and the second associated photodetector at opposite ends of said active area and having a two-dimensional shape as the pixel array is viewed from above"**, as exhibited in figure 6.

In addition, Hashimoto discloses, **"a common output for charges (55) generated from the first photodetector and the second photodetector at a portion of said active area between said first and second photodetectors, the common output being coupled to a signal output line shared by the first pixel and the second pixel"**, as exhibited in figure 6.

However, Hashimoto and Bird fail to explicitly disclose an active area component that extends diagonally with respect to an extending direction of said signal output line.

Therefore because Hashimoto and Bird either alone or combination fail to teach every limitation of claim 113, claim 113 is allowable.

Regarding claim 114, because Hashimoto and Bird fail to disclose all the limitations of claim 113, dependent claim 114 is also allowable.

Regarding claims 115 and 117, claims 115 and 117 contain similar limitations to claim 113 and are allowable for the same reasons as stated above (see claim 113).

Regarding claims 116 and 118-123, because claims 116 and 118-123 are dependent from one of allowable claims 113, 115, and 117, claims 116 and 118-123 are also allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL BERARDESCA whose telephone number is

(571)270-3579. The examiner can normally be reached on Mon- Fri 8:30am-6:00pm EST (Alternate Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571)272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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1/28/2010